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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WONG, LINDA	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,693	CAO, JUN	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Drawings

1. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.
2. The drawings were received on 3/15/2005. These drawings are accepted by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1,2,3,4,7-11,13,16-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge (US Patent No.: 4535459) in view of Spagnoletti et al (US Patent No.: 6151356).
   a. **Claim 1**, In the applicant's arguments to the rejection of claim 1, the applicant states Hogge does not disclose a second signal is not produced by a latch, but produced by a flip-flop. (page 17 of Applicant's Arguments) Although Hogge does not explicitly state the second signal is outputted by a latch, based on the Spangoletti et al's invention, it can be shown that the second signal is indeed outputted by a latch. Spangoletti et al discloses the second signal (Fig. 4,

output from label 203) is outputted when the clock signal (Fig. 4, label inverse CLOCK) is at the first level and stored at the second signal. (Col. 12, lines 33-37) Spangoletti et al's shows in Fig. 4, labels 202 and 203, the difference between these two logic gates, flip-flop 202 and latch 203, is the inverted clock controlling the latch. In Fig. 5, a diagram of the clock output of Q203 depicts the latch outputting a delayed signal of the flip-flop, Q202, which is the basic functionality of a latch. Comparing this portion of Spangoletti et al's invention to Hogge's invention, in Fig. 4, label 116, Hogge discloses a logic gate is depicted exactly the same as Spangoletti et al's invention in Fig. 4, label 203. Also, Hogge shows in Fig. 5a, label 122, the output of the logic gate found in Fig. 4, label 116, a delayed signal of the output from label 112 found in Fig. 4 and 5a.

b. **Claim 2**, Although Hogge does not disclose a reference and phase signal inputted into a loop filter, Spagnoletti et al discloses a reference and phase signal inputted in to a loop filter. (Fig. 11, labels 602 and 603)

c. **Claims 3,4,7-11,13,16-18** are rejected as found in the previous office action.

   i. Regarding **claim 3**, line 1, Hogge Jr. discloses a first storage device (Fig. 4, label 102) as a flip-flop and a second storage device (Fig. 4, label 116) as a latch.

   ii. Regarding **claim 4,** line 1, Hogge Jr. discloses two XOR gates that are used to provide an error and reference signal (Fig. 4, label 106 and 114).

   iii. Regarding **claim 7,** line 1, Hogge Jr. discloses a first storage device (Fig. 4, label 102) that receives and stores the data signal (Fig. 4, label 100) to generate the first signal (Fig. 4, label 112), a second storage device (Fig. 4, label 116) that receives and stores the first signal (Fig. 4, label 112) to generate a second signal (Fig. 4, label 122), a delay block (Fig. 4, labels 104 and 105 and 108 and 110) that receives and delays the data signal to

produce a third signal (Fig. 4, input to 106 from 105), a logic circuit (Fig. 4, label 106) configured to combine the first and second signal and a logic circuit (Fig. 4, label 114) that can combine the first and third signal (Fig. 4, label 112 and input to 106 from 105).

iv. **Claim 8** inherits all the limitations of claim 3.

v. Regarding **claim 9,** line 1, Hogge Jr. discloses a flip-flop and a latch receiving a clock signal. It is inherent in the prior art that a clock signal would comprise of edges, first and second levels. (Fig. 4, label 102 and 116)

vi. Regarding **claim 10**, line 1, Hogge discloses a flip-flop that stores the data on the first edge and the latch latches on the second level (Fig. 5a, labels 100, 124, 105, 126).

vii. Regarding **claim 11**, line 1, Hogge discloses a first edge that is falling and a second edge that is rising (Fig. 5a, label 126).

viii. Regarding **claim 13**, line 1, Hogge discloses a flip-flop (Fig. 4, label 102) receiving a data input port (Fig. 4, label 100) and a clock input (Fig. 3, label 82 and 84) coupled to a clock port (Fig. 3, label 78), a latch (Fig. 3, label 50), in the form of a flip-flop, which performs the functionalities of a latch, having a data input coupled to an output of the first flip-flop (Fig. 3, label 48) and a clock input coupled to the clock port (Fig. 3, label 82), a delay element having an input coupled to the data input port (Fig. 4, labels 100, 104, 108, 105, 110), a first logic circuit (Fig. 4, label 106) having a first input coupled to the output of the flip-flop (Fig. 4, label 112) and a second input coupled to the output of the latch (Fig. 4, label 112) and a second logic circuit (Fig. 4, label 114) having a first input coupled to the output of the first flip-flop (Fig. 4, label 112) and a second input coupled to the output of the delay element. (Fig. 4, label 112)

- Regarding the applicant's arguments to claim 13, the rejection of claim 13 remains the same due to claim 13 does not recite how the latch functions, but only how the latch is connected. Hogge discloses a flip-

flop, which performs the functionality of a latch and is connected as recited in the claim.

ix. **Claims 16 -18** inherits all the limitations of claim 4.

4. **Claims 5, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge (US Patent No.: 4535459) in view of Spagnoletti et al (US Patent No.: 6151356) and further in view of Bowles (Publication: Chapter7).

   a. **Claim 5**, Although Hogge does not explicitly disclose the delay of the first signal is approximately equal to the clock-to-Q delay of the flip flop, it is obvious to one skilled in the art to synchronize the data input with the output from the flip-flop to prevent races or spikes when the data input is combined with the output of the flip-flop.

   b. **Claim 12** inherits all the limitations of claim 5.

5. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge (US Patent No.: 4535459) in view of Spagnoletti et al (US Patent No.: 6151356) and further in view of Bowles (Publication: Chapter7) and further in view of Evans (US Patent No.: 3631488).

   a. **Claim 6**, Although Hogge, Spagnoletti et al, Bowles do not disclose a flip-flop comprising inductors as loads, Evans discloses a flip-flop with inductive loads. (Col. 5, lines 38-42 and Fig. 3, label 228)

6. **Claims 14,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge (US Patent No.: 4535459) in view of Spagnoletti et al (US Patent No.: 6151356) and further in view of Meghelli (US Patent No.: 6577694).

   a. **Claims 14 and 15**, Although Hogge and Spagnoletti et al do not disclose a phase detector receiving differential signals, Meghelli discloses a phase detector receiving differential inputs. (Col. 3, lines 5-26)

7. **Claims 19-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge (US Patent No.: 4535459) in view of Spagnoletti et al (US Patent No.: 6151356) and further in view of Wang et al (US Patent No.: 6219380).

   a. **Claims 19, 20 and 21**, Although Hogge, Spanoletti does not disclose an optical receiver, Wang et al discloses an optical receiver coupled to the optical transmitter (Fig. 1, label To photo TX-Rear end and From photo Rx-Front End), wherein receiving and transmitting comprises a light emitting diode for transmitting (Col. 2, lines 12-14), a photo-diode for receiving (Col. 2, lines 14-16), a receiver amplifier coupled to the photo diode (Col. 2, lines 16-18) and a phase detector coupled to the receiver amplifier (Fig. 1, label 162 and 192).

Allowable Subject Matter

8. **Claims 22-23** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW

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